AMENDMENTS TO THE ABSTRACT:

Please replace the Abstract with the following amended Abstract:

ABSTRACT OF THE DISCLOSURE

An active matrix substrate of a channel protection type having a gate electrode, a drain electrode and a pixel electrode is isolated ~~from one another from layer to layer~~ in each layer by insulating films. The active matrix substrate is to be prepared by four masks. A gate electrode layer, a gate insulating film and an a-Si layer are processed to the same shape on a transparent insulating substrate to form a gate electrode layer ~~(102 of Fig.6)~~ and a TFF area. A drain electrode layer ~~(106 of Fig.6)~~ is formed by a first passivation film ~~(105 of Fig.6) via a~~ with the first passivation film ~~(105 of Fig.6)~~ formed as an upper layer. In a second passivation ~~film (107 of Fig.6)~~ film, formed above ~~it~~ the first passivation film, are bored ~~an~~ a first opening through the first and second passivation films and ~~an~~ a second opening through the second passivation film. A wiring connection layer is formed by ITO ~~(108 of Fig.6)~~ provided as an uppermost layer. A storage capacitance unit, ~~comprised of~~ including the first and second passivation films sandwiched between the gate electrode and an electrode layer formed as a co-layer with respect to the gate electrode, is ~~provided in~~ connected to the pixel electrode.

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An active matrix substrate of a channel protection type having a gate electrode, a drain electrode and a pixel electrode is isolated in each layer by insulating films. The active matrix substrate is to be prepared by four masks. A gate electrode layer, a gate insulating film and an a-Si layer are processed to the same shape on a transparent insulating substrate to form a gate electrode layer and a TFF area. A drain electrode layer is formed by a first passivation film with the first passivation film formed as an upper layer. In a second passivation film, formed above the first passivation film, are bored a first opening through the first and second passivation films and a second opening through the second passivation film. A wiring connection layer is formed by ITO provided as an uppermost layer. A storage capacitance unit, including the first and second passivation films sandwiched between the gate electrode and an electrode layer formed as a co-layer with respect to the gate electrode, is connected to the pixel electrode.